Rpp 00 W 000 14

INVENTION DISCLOSURE FORM

(Please print or type)

1. Descriptive title of the invention: METHOD FOR CONSTRUCTING A WAFER INTERPOSER BY USING B-STAGE LAMINATES

2. Invention submitted by:

(a) Name JOHN (first) PIERCE (last) (middle)
Employee # _____ Department TIDC Group _____
Employment Status: [X] Employee [ ] Subcontractor

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Phone 972-512-1912 Fax 972-512-1933 E-mail jpierce@micro-asi.com
Home: Address 7019 WESTER WAY DALLAS TX 75248
Phone 972-931-6989 Fax _____
Country of citizenship US
Supervisor JERRY KLINE (name) TIDC (location) 972-512-1905 (phone number)

(b) Name _____ (first) (middle) (last)
Employee # _____ Department _____ Group _____
Employment Status: [ ] Employee [ ] Subcontractor
Work: Address _____
Phone _____ Fax _____ E-mail _____
Home: Address _____
Phone _____ Fax _____
Country of citizenship _____
Supervisor _____ (name) (location) (phone number)

(If there are more than two inventors, please include additional sheets so that the above information is provided for all inventors)

3. History of invention
Date and location invention was first conceived 9/1/00 TIDC
Date first sketch or drawing was made 9/1/00 [ ] Not yet started
Date construction or model was started _____ [X] Not yet started
Date construction or model was completed _____ [X] Not yet complete
Date testing was started _____ [X] Not yet started
Date successful testing was completed _____ [X] Not yet complete

4. Was any of the work performed under or in preparation of a government contract? [ ] Yes [X] No

5. Has there been any experimental use of the invention? [ ] Yes [X] No

Has there been any er to sell, sale or production use of the vention? Γ Yes ☒ No
Is sale or production use presently scheduled? Γ Yes ☒ No
If any answers are "yes," please explain giving dates and circumstances _____

6. (a) Has there been any disclosure of the subject matter of this invention outside the company or is such disclosure anticipated? Γ Yes ☒ No

(b) Has the subject matter of this invention been included in any publication, such as catalogs, advertising materials, data books, application notes, conference papers, magazine articles, government or customer proposals, or is any such disclosure anticipated? Γ Yes ☒ No

If your answer was Ayes,≅ please explain giving dates and details of publication _____

7. Please provide a brief written summary of the invention and attach any sketches, diagrams, drawings, prints, photographs, etc. which will aid in understanding this invention. Each of the points set forth below should be included in the written description:

(a) A brief discussion of the problem(s) solved by the present invention.
(b) A list and discussion of known prior art, including the manner in which others have attempted to solve the problem(s) and the disadvantages and weaknesses in the prior art solutions. (Specify any literature references or patents available.)
(c) A specific embodiment of the invention including the important features of the invention believed to be novel along with the advantages of the invention over the prior art solutions.

8. Signatures of the Inventors:

(a) John T Rief Date SEPT 14, 2000

(b) _____ Date _____

9. Signatures of the Witnesses:
We, the undersigned, have read and understood this disclosure:

Name (typed or printed)	Signature	Date
Name (typed or printed)	Signature	Date

METHOD FOR CONSTRUCTING

A WAFER INTERPOSER

BY USING B-STAGE LAMINATES

JOHN PIERCE

September 14, 2000

BACKGROUND:

Previous disclosures have described techniques for building a wafer interposer. These disclosures have also provided information regarding the cost and performance advantages of a wafer interposer as contrasted to traditional semiconductor backend packaging practices. Each of the previously disclosed inventions described a substrate that is connected to a wafer to form a wafer interposer. Implementing a wafer in this fashion requires that the substrate be very coplanar (flat).

Because of the very precise and costly manufacturing methods used to create a semiconductor wafer, it can, for all practical purposes, be considered to be flat. Typical substrate materials, however, are much less coplanar. A laminate substrate may have variances up to .005 in./in. A total variance of .04 inch could be expected across an 8 inch wafer. If the substrate is connected to the wafer using solder, then this solder connection would be required to compensate for the height variances in the substrate. Because of the geometries of the pads on the wafers, a maximum solder ball height of approximately .01 inch is possible. Therefore, only those solder bumps that resided on the highest part of the substrate would make contact with the wafer.

In the above example, the coplanarity of the substrate would have to be less than .00125 in./in. (.01 in across 8 inches) in order for all pads of the wafer to be contacted by the substrate. This requirement increases the cost of the substrate. As geometries become tighter, solder bump height decreases. Wafers are also becoming larger (e.g. 300mm = 12 inches across). These two factors increase the coplanarity or flatness requirements of the substrate which increases the cost of the substrate.

The invention described here overcomes the coplanarity problem by building the interposer onto the wafer. The substrate material is malleable at the time that it is placed on the wafer. Therefore, it can be urged against all contact pads on the wafer. Later, the entire assembly is cured. During the cure process solder contacts are made. Additionally, the underfill used to stabilize the assembly is cured at this time.

DESCRIPTION OF THE INVENTION:

Figure 1 shows the topside of a substrate 10. There are contact pads on both sides of the substrate. The pads that will contact the wafer are on the bottom and are not shown in Figure 1. These pads on the bottom are arranged to be in a mirror image of the pads on the wafer. They will typically have smaller geometries and tighter pitches than the pads shown on the top.

Figure 1 shows contact pads 11 that connect to four individual circuits 12 or die on the wafer. Each die has nine pads. Each contact pad on the bottom of the substrate 10 is connected to a pad 11 on the topside of the substrate. Although Figure 1 shows a die with nine pads, an actual semiconductor die may have many more individual contact pads (as many as 2000 or more). The pads 11 on the topside are constructed in an array with geometries larger than the pads on the bottom. This is done to enable easy contact with external burn-in or electrical test equipment. It also allows the use of less expensive printed circuit boards for attachment of individual circuits after the circuits have been fully processed and diced.

It is important to note that the substrate of Figure 1 has not been attached to the wafer. The material of the substrate is a laminate containing partially cured resins. This is often referred to as "B stage" laminate. The conducting pads on the top and bottom of the substrate can be copper, gold or other suitable conductive metal. They can also be a compound of different metals.

Figure 2 shows a wafer prepared for connection to the substrate. Solder bumps 21 have been applied to wafer 20. There will be one unique solder bump for each contact pad on the wafer. The solder bump may be applied directly to the die contact pad. Often the die pad will require additional layers of metal to be applied prior to the application of the solder bump. This is necessary to insure that the solder bump makes a strong and reliable connection to the die pad.

Additional metalization may be added to the wafer prior to the application of the solder bumps that redistribute the die contact pads. This is often necessary if the die pads have very small geometries or very close pitches. The redistributed pads help ensure that the solder connections made between the wafer and the substrate are robust and reliable.

Also shown in Figure 2 is no flow underfill 22. The purpose of this underfill is to stabilize the assembly by resisting any lateral forces caused by the differences between thermal expansion of the wafer and the substrate. The underfill is applied over the entire wafer but is not cured.

Figure 3 shows the substrate and the wafer prior to assembly into a wafer interposer. At this point the substrate 10 still contains partially cured resins. The solder bumps 21 have been applied to the contact pads of each die on wafer 20, The no flow underfill 22 is not cured at this step.

Prior to assembly, the wafer 20 is placed on a flat surface 31. The wafer is held in place by vacuum or other suitable technique. The substrate 10 is also held in place against a flat surface 32. A suitable compound is used to coat the surface of the substrate 10 that is in contact with the flat surface 32. This prevents the substrate from adhering to the flat surface during the curing process. Flat surfaces 31 and 32 as illustrated in Figure 3 can be various configurations and materials. The primary requirement of the surface is that it is as coplanar as the wafer. Also, not shown is a mechanism that can bring the surfaces together. This mechanism will be obvious to those skilled in the art. The mechanism must be able to adjust the position of the substrate or the wafer in order to perfectly align the contact pads on the substrate 10 with the solder bumps 21 on the wafer 20. Alignment is accomplished using split vision optics or any other suitable technique.

Prior to final assembly, the flat surface 32 may be heated to insure that the substrate 10 is in a malleable condition. The heating can be accomplished using forced heated air, heating coils or other method generally known in the industry.

Figure 4 shows the interposer assembly during assembly. Flat surfaces 32 and 31 are brought together by mechanical mechanisms not shown such that all solder bumps 21 contact the pads on substrate 10. A method for insuring that 100% contact is made is to compress the solder bumps. For example, if the solder bump is nominally .006 in. high, then the surfaces would be brought together such that the resulting solder bump would only be .005 in. high. This would compensate for any and all variances in the coplanarity of the substrate, wafer, solder bumps and flat surfaces.

Another method of manufacture includes applying underfill and solder bumps to the substrate instead of the wafer. Additionally, underfill and solder bumps may be applied to both the wafer and the substrate. The particular geometries of the contact pads or characteristics of the wafer or substrate would dictate the preferred method.

Figure 5 shows a "before" and "after" example of the effect of compression to make 100% connection. Before compression takes place, solder bumps 50a and 50b are not making contact with substrate 10. If the entire assembly were cured at this stage, missing connections would be present. Bringing the flat surfaces closer together results in the "after" configuration in Figure 5. Here, solder bumps 50a and 50b are making contact with substrate 10. The other solder bumps are compressed to allow 50a and 50b to contact the substrate. As they are compressed, solder must expand as height is reduced. This is possible because the surrounding underfill is not yet cured. The amount of compression to be applied will vary with each individual application.

After the wafer and substrate are properly joined, the entire assembly is cured. This curing can take place while the assembly continues to be held by the flat surfaces. Alternatively, the wafer and substrate may be removed from the surfaces and cured. During the curing process, the substrate and underfill become fully cured. In addition, the solder bumps make permanent contact with the contact pads. After the curing process, testing, burn-in or other processes designed to determine the merit of each circuit may be performed. The last step is dicing the assembly into individual circuits.

The invention described uses solder as a method of achieving connection. Other materials such as conductive polymer, conductive plastic or other suitable conductive material may be used.

The interposer may also be constructed by adding additional layers of substrate. This may be necessary to achieve thicker packages or to add additional interconnect options such as power and ground planes.

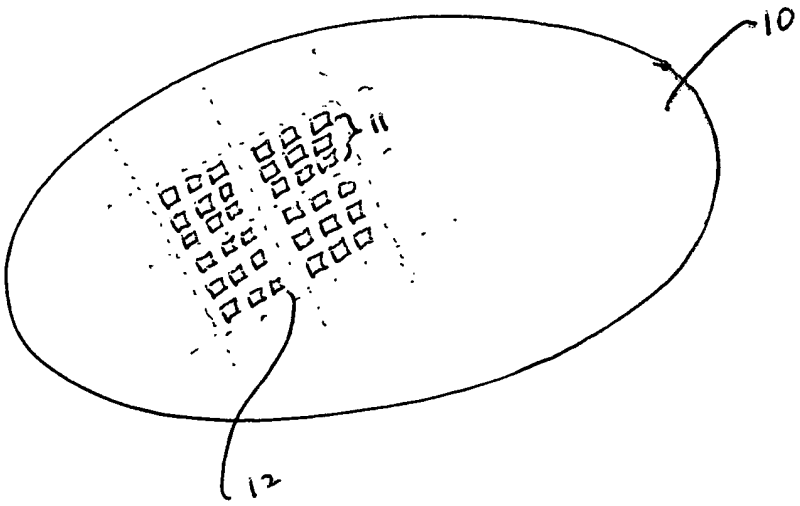


FIGURE 1

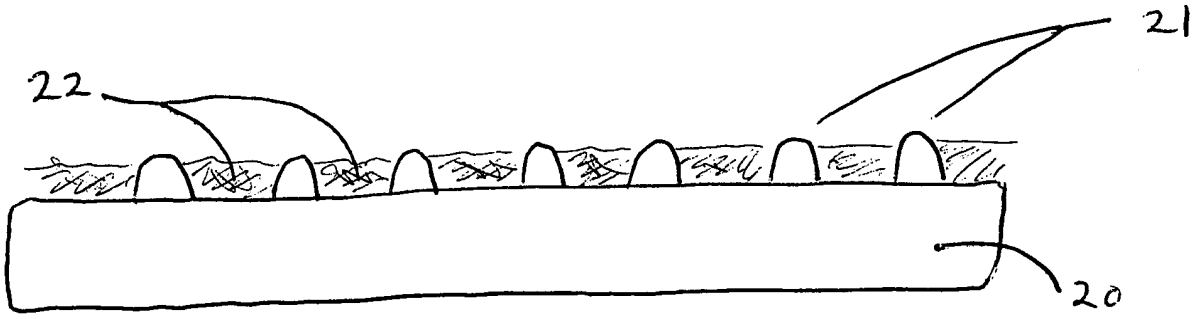


FIGURE 2

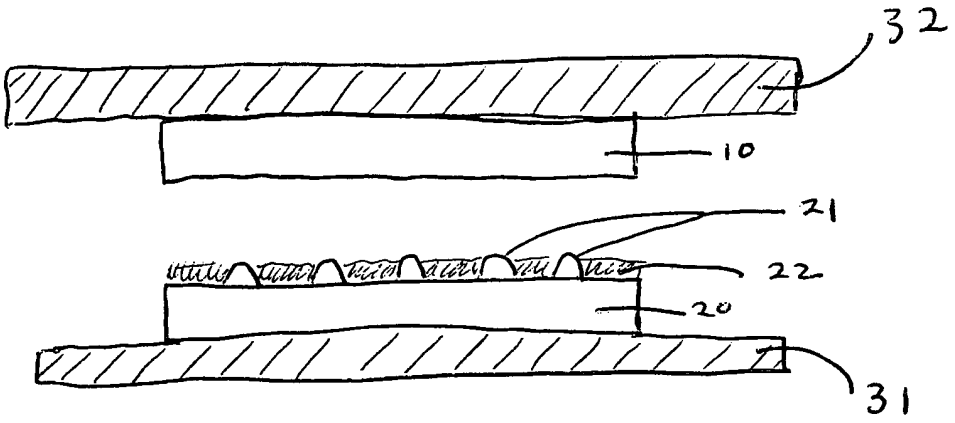


FIGURE 3

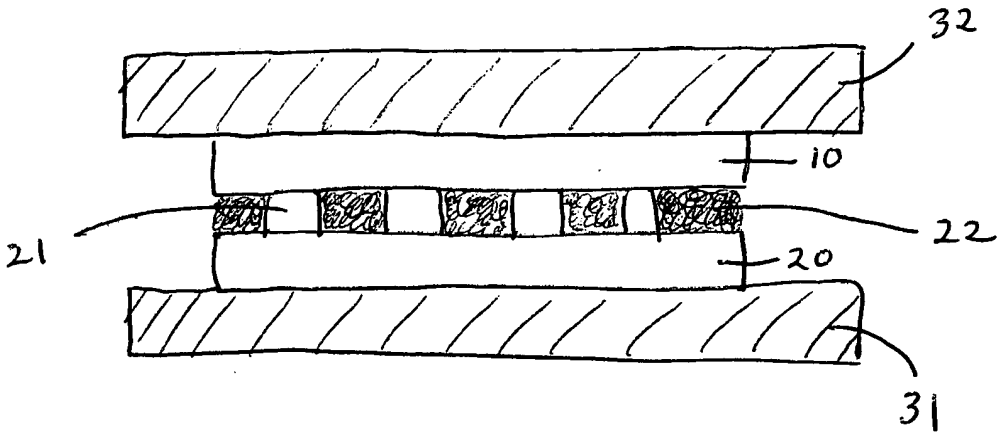
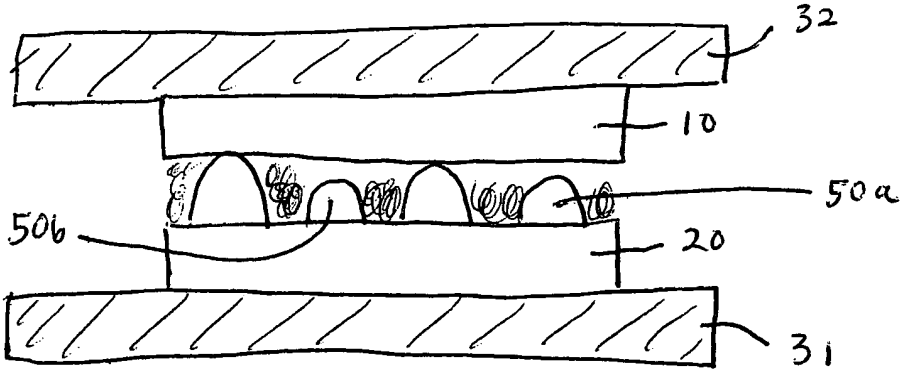
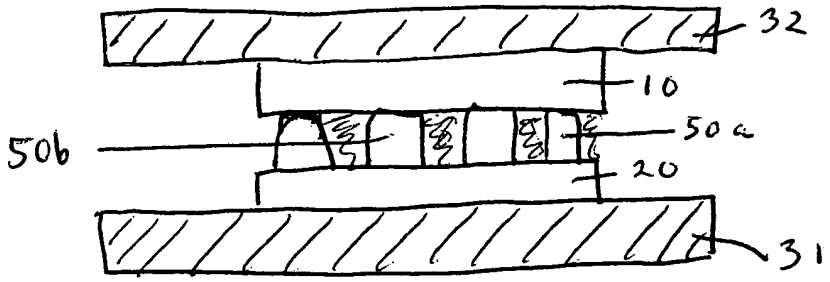


FIGURE 4



BEFORE



AFTER

FIGURE 5

GARDERE & WYNNE, L.L.P.
ATTORNEYS AND COUNSELORS

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011 (525) 546-8030

October 5, 2000

Mr. John Pierce
Micro-ASI, Inc.
1440 MacArthur Mills Dr.
Suite 100
Carrollton, TX 75007

Re: Results of Patent Search: "Method for Constructing a Wafer Interposer by Using B-Stage Laminates"
Our File No.: 121251-12

Dear John:

As requested we have conducted a patent search for issued US patents that relate to a "Method for Constructing a Wafer Interposer by Using B-Stage Laminates." It is our understanding that this invention uses a B-Stage laminate between the wafer and substrate to compensate for coplanarity problems and improve solder connections.

Copies of the patents identified in our search are enclosed for your consideration. While the patents we discovered disclose some of the aspects of the invention, none of the patents identified herein appear to disclose all of the features as we currently understand them. The following patents were discovered in the search:

U.S. No.	Issue Date	Inventor	Title
3,939,558	Feb. 24,1976	Riley	Method of Forming an Electrical Network Package
5,086,558	Feb. 11, 1992	Grube, et al.	Direct Attachment of Semiconductor Chips to a Substrate with a Substrate with a Thermoplastic Interposer
5,489,804	Feb. 6, 1996	Pasch	Flexible Preformed Planar Structures for

			Interposing Between a Chip and a Substrate
5,635,010	Jun. 3, 1997	Pepe, et al	Dry Adhesive Joining of Layers of Electronic Devices
5,802,713	Sep. 8, 1998	Deamer	Circuit Board Manufacturing Method
5,936,847	Aug. 10, 1999	Kazle	Low Profile Electronic Circuit Modules

U.S. Patent No. 3,939,558 discloses an electrical network package in which B-Stage adhesive material is sandwiched between a substrate bearing numerous electrical circuit elements, and a protective superstrate. The package is first heated to initiate gel formation. It is then cooled and momentarily compressed to secure adhesion.

U.S. Patent No. 5,086,558 discloses a method of joining semiconductor chips to substrate using flip chip techniques in conjunction with a thermoplastic interposer. The interposer is fabricated separately with vias corresponding to contact patterns of the chips built in. The connection between the solder bumps is accomplished with the addition of conductive attachment material into the vias.

U.S. Patent No. 5,489,804 discloses a preformed flexible interposer made of thermoplastic material. Vias are built into the interposer to correspond with the contact patterns of the chips. The vias align the solder bumps so that they can fused together.

U.S. Patent No. 5,635,010 discloses the use of adhesives with "good B-Stage properties" to bond layers of electronic devices into an integral stack. The adhesive is coated onto the wafers, which are then stacked and bonded, or sliced and then stacked to form suitable fixtures.

U.S. Patent No. 5,802,713 discloses a circuit board manufacturing procedure that involves the application of B-Stage semi-cured material to a printed circuit board before machine soldering. The presence of the semi-cured material retards heat, reduces the incidence of hot and cold spots, and reduces the movement of thermal pads during soldering.

U.S. Patent No. 5,936,847 discloses a method for circuit module construction that entails sandwiching a layer of non-conductive polymeric material between the electronic components and the substrate. The polymer acts as adhesive and underfill. The substrate and underfill have apertures that are aligned with signal traces, and the apertures are filled with conductive polymer to establish a connection.

Although we have made every effort to ensure that the search is thorough, no search can ever be completely exhaustive. The search included issued patents, and was focused on areas of technology that we believe to be most closely related to the subject matter of your invention. Due to limitations inherent in any searching methodology, however, you should be aware that it

is possible that a patent examiner may uncover and cite an undiscovered reference during the course of prosecution.

Please note that although no single aforementioned patent discloses the Method for Constructing a Wafer Interposer Using B-Stage Laminates in its entirety, the aforementioned patents do disclose the many of the elements as we understand them. As a result, limited patent protection may be available for the Method for Constructing a Wafer Interposer Using B-Stage Laminates. After your review of the above-identified patents and the brief overview presented herein, please instruct me on how you would like to proceed. In the meantime, if you have any questions or comments, please feel free to give me a call.

Very truly yours,

GARDERE & WYNNE, L.L.P.

Sanford E. Warren, Jr.
SEW:TCW

Enclosures

cc: David Segrest (w/o encl.)
Daniel J. Chalker (w/o encl.)
Thomas C. Wright (w/o incl.)

Attorney Docket No.: 1384-1023

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application: John L. Pierce

Serial No.: 09/738,193

Filed: December 15, 2000

Art Unit: 2827

Examiner: David E. Graybill

For: Method for Producing a Semiconductor Wafer-Interposer

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Declaration of Daniel J. Chalker

Dear Sir:

I, Daniel J. Chalker, hereby declare the following:

1. From May 1998 to September 2002, I was employed at Gardere Wynne Sewell, LLP (previously Gardere & Wynne, LLP) (hereinafter referred to as "Gardere") in the Intellectual Property Group.

2. As part of my responsibilities at Gardere, I oversaw the preparation and filing of patent applications including numerous applications for the inventor Mr. John L. Pierce of Micro-ASI, Inc. (hereinafter referred to as "Micro-ASI").

3. I attended a regularly scheduled patent committee meeting on or about September 21, 2000 at which Gardere attorneys and representatives of Micro-ASI were present. I received a disclosure of the invention described in the above-captioned patent application at the meeting.

4. I oversaw the completion of a patentability search on the invention described in the above-captioned patent application between September 21, 2000 and October 5, 2000.

5. I attended a regularly scheduled patent committee meeting on or about October 5, 2000 at which Gardere attorneys and representatives of Micro-ASI were present. The results of the patentability search were presented to the representatives of Micro-ASI at the meeting.

6. I attended a regularly scheduled patent committee meeting on or about October 19, 2000 at which Gardere attorneys and representatives of Micro-ASI were present. The representatives of Micro-ASI granted approval for the preparation and filing of the above-captioned patent application at the meeting.

7. I oversaw the completion of a draft of the above-captioned patent application between October 19, 2000 and November 30, 2000.

8. I attended a regularly scheduled patent committee meeting on or about November 30, 2000 at which Gardere attorneys and representatives of Micro-ASI were present. A draft of the above-captioned patent application was presented to the representatives of Micro-ASI for review by the inventor at the meeting.

9. I oversaw the completion of the approved draft application, preparation of the formal drawings and preparation of the Declaration and Power of Attorney between November 30, 2000 and December 15, 2000.

10. I oversaw the filing of the patent application on December 15, 2000.

11. Based upon my experience as a patent attorney having drafted, overseen and/or filed over 100 patent applications, I believe that Mr. Pierce, Micro-ASI and Gardere diligently prepared and filed the above-captioned patent application following Mr. Pierce's

conception of the invention on or about September 1, 2000.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Daniel J. Chalker

8/23/2004
Date

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe that I am the original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **"System, Method and Apparatus for Constructing a Semiconductor Wafer-Interposer Using B-Stage Laminates"** the specification of which:

_X_ is attached hereto.

___ was filed on _____ as Application Serial No. _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application of which priority is claimed:

Prior Foreign Application(s)		Priority Claimed
_____ (Number)	_____ (Country)	_____ _____ _____ (Day/Month/Year Filed)
_____ (Number)	_____ (Country)	_____ _____ _____ (Day/Month/Year Filed)

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States Application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I hereby acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

_____ (Appl.Ser.No.)	_____ (Filing Date)	_____ (Status: patented, pending, abandoned)

(Appl.Ser.No.) (Filing Date) (Status: patented, pending, abandoned)

POWER OF ATTORNEY: As named inventor, I hereby appoint the following attorney(s) jointly and severally to prosecute this application and transact all business in the Patent and Trademark Office connected therewith and to file any and all International Application(s) with respect thereto and to act on my behalf before the competent International Authorities with respect thereto: Sanford E. Warren, Jr. (Reg. No. 33,219), Daniel J. Chalker (Reg. No. 40,552), Edwin S. Flores (Reg. No. 38,453), Kay Lyn Schwartz (Reg. No. 39,020), Theodore F. Shiells, (Reg. No. 31,569), Lawrence R. Watson (Reg. No. 31,891), Matthew Burr (Reg. No. 37,591), Kenneth Emanuelson (Reg. No. 46,684), Madeleynne Farber (Reg. No. 45,410) and Todd Landis (Reg. No. 44,200).

SEND CORRESPONDENCE TO:

Daniel J. Chalker
Gardere Wynne Sewell L.L.P.
3000 Thanksgiving Tower
1601 Elm Street
Dallas, TX 75201-4761

DIRECT TELEPHONE CALLS TO:

Daniel J. Chalker
(214) 999-4785
(214) 999-3785 (FAX)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of first inventor: John L. Pierce

Inventor's signature John L Pierce 12/14/00
Date

Residence: 7019 Wester Way
Dallas, Texas 75248

Citizenship: United States

Post Office Address: Same as above

GARDERE

attorneys and counselors ▪ www.gardere.com

Writer's Direct Dial 214-999-4785
Direct Fax 214-999-3785
dchalker@gardere.com

December 15, 2000

BOX NEW APP/FEE
Assistant Commissioner for Patents
Washington, D.C. 20231

VIA EXPRESS MAIL NO. EL417462232US

Re: Patent Application for "System, Method And Apparatus For Constructing A Semiconductor Wafer-Interposer Using B-Stage Laminates"
Our File No.: 121251-1016

Dear Sir:

Enclosed for filing for the above referenced patent application, please find the following:

(1) Patent Application;
(2) Transmittal Form;
(3) Check for $552.00;
(4) Declaration/Power of Attorney; and
(5) Return Postcard.

Please file the above documents and return the file-stamped postcard to our offices.

Thank you for your assistance. Should you have any questions, please call me.

Respectfully submitted,

GARDERE WYNNE SEWELL, LLP.

Daniel J. Chalker
Registration No. 40,552

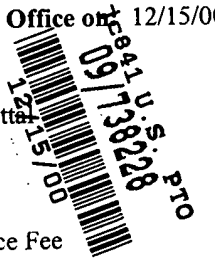
DJC/hrh

Enclosures
cc: Sanford E. Warren, Jr.

DALLAS 954754v1

Attorney(s): DJC/hh
Client/Matter#: 121251-1016
Title: System, Method And Apparatus For Constructing A SEmiconductor Wafer-Interposer Using B-Stage Laminates
Inventor(s): John Pierce
Today's Date: 12/15/00 **Due Date:**

Check Amount: $552.00
Serial/Patent No.:
Filed with U. S. Patent Office on: 12/15/00



APPLICATION FOR PATENT [Check all items that apply]:

- ☒ Spec pages 20 ☒ Claims
- ☒ Drawings 2 Sheets
- ☒ Declaration ☐ Oath ☒ Power
- ☐ Verified Statement
- ☐ Assignment
- ☐ Continuation ☐ Divisional
- ☐ CIP Application
- ☐ Preliminary Amendment
- ☐ Information Disclosure Statement
- ☐ Amendment
- ☐ Amendment Under Rule 1.312
- ☐ Amendment After Final

GARDERE WYNNE SEWELL LLP

JAN 04 2001

- ☐ Issue Fee Transmittal
- ☒ Letter
- ☐ Notice of Appeal
- ☐ Brief
- ☐ Patent Maintenance Fee
- ☐ Petition:
- ☐ Response
- ☐ Status Request
- ☒ Other: Postcard
- ☒ Express Mail EL417462232US
- ☐ Certificate of Mailing
- ☐ First Class Mail

DOCKETED

Attorney Docket No.: 1384-1023

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application: John L. Pierce

Serial No.: 09/738,193

Filed: December 15, 2000

Art Unit: 2827

Examiner: David E. Graybill

For: Method for Producing a Semiconductor Wafer-Interposer

Mail Stop Non-Fee Amendment
Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Declaration Under 37 C.F.R. §1.131

Dear Sir:

This is a Declaration under 37 C.F.R. §1.131 to establish invention of the subject matter of the above-captioned application in the United States at a date prior to November 9, 2000, i.e., the effective date of the cited prior art United States Patent No. 6,400,019, entitled "Semiconductor Device with Wiring Substrate," issued in the names of Hirashima et al., (hereinafter "Hirashima").

To establish the date of invention of the subject matter of the above-captioned application, a copy of a disclosure form entitled "Method for Constructing a Wafer Interposer by Using a

B-Stage Laminates" and a copy of a disclosure document entitled "Method for Constructing a Wafer Interposer by Using a B-Stage Laminates" are attached hereto and submitted as evidence as Exhibit A and Exhibit B, respectively. Based on these documents, it can be seen that the invention in this application was made at least by the date of September 14, 2000, which is a date earlier than the effective date of the reference.

As the below named inventor, I hereby declare that the completion of the invention was diligent, from the time of my conception, to a time just prior to the date of Hirashima, up to the filing of this application on December 15, 2000.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

John L. Pierce, Inventor

March 10, 2004
Date

00W00014

INVENTION DISCLOSURE FORM

(Please print or type)

1. Descriptive title of the invention: METHOD FOR CONSTRUCTING A WAFER INTERPOSER BY USING B-STAGE LAMINATES

2. Invention submitted by:

(a) Name JOHN (first) PIERCE (last) (middle)
Employee # _____ Department TIDC Group _____
Employment Status: [X] Employee [ ] Subcontractor

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(b) Name _____ (first) (middle) (last)
Employee # _____ Department _____ Group _____
Employment Status: [ ] Employee [ ] Subcontractor
Work: Address _____
Phone _____ Fax _____ E-mail _____
Home: Address _____
Phone _____ Fax _____
Country of citizenship _____
Supervisor _____ (name) (location) (phone number)

(If there are more than two inventors, please include additional sheets so that the above information is provided for all inventors)

3. History of invention
Date and location invention was first conceived 9/1/00 TIDC
Date first sketch or drawing was made 9/1/00 [ ] Not yet started
Date construction or model was started _____ [X] Not yet started
Date construction or model was completed _____ [X] Not yet complete
Date testing was started _____ [X] Not yet started
Date successful testing was completed _____ [X] Not yet complete

4. Was any of the work performed under or in preparation of a government contract? [ ] Yes [X] No

5. Has there been any experimental use of the invention? [ ] Yes [X] No

Has there been any er to sell, sale or production use of the vention? Γ Yes ☒ No
Is sale or production use presently scheduled? Γ Yes ☒ No
If any answers are "yes," please explain giving dates and circumstances _____

6. (a) Has there been any disclosure of the subject matter of this invention outside the company or is such disclosure anticipated? Γ Yes ☒ No

(b) Has the subject matter of this invention been included in any publication, such as catalogs, advertising materials, data books, application notes, conference papers, magazine articles, government or customer proposals, or is any such disclosure anticipated? Γ Yes ☒ No

If your answer was Ayes,≅ please explain giving dates and details of publication _____

7. Please provide a brief written summary of the invention and attach any sketches, diagrams, drawings, prints, photographs, etc. which will aid in understanding this invention. Each of the points set forth below should be included in the written description:

(a) A brief discussion of the problem(s) solved by the present invention.
(b) A list and discussion of known prior art, including the manner in which others have attempted to solve the problem(s) and the disadvantages and weaknesses in the prior art solutions. (Specify any literature references or patents available.)
(c) A specific embodiment of the invention including the important features of the invention believed to be novel along with the advantages of the invention over the prior art solutions.

8. Signatures of the Inventors:

(a) John T Rief Date SEPT 14, 2000

(b) _____ Date _____

9. Signatures of the Witnesses:
We, the undersigned, have read and understood this disclosure:

Name (typed or printed) Signature Date

Name (typed or printed) Signature Date

METHOD FOR CONSTRUCTING A WAFER INTERPOSER BY USING B-STAGE LAMINATES

JOHN PIERCE

September 14, 2000

BACKGROUND:

Previous disclosures have described techniques for building a wafer interposer. These disclosures have also provided information regarding the cost and performance advantages of a wafer interposer as contrasted to traditional semiconductor backend packaging practices. Each of the previously disclosed inventions described a substrate that is connected to a wafer to form a wafer interposer. Implementing a wafer in this fashion requires that the substrate be very coplanar (flat).

Because of the very precise and costly manufacturing methods used to create a semiconductor wafer, it can, for all practical purposes, be considered to be flat. Typical substrate materials, however, are much less coplanar. A laminate substrate may have variances up to .005 in./in. A total variance of .04 inch could be expected across an 8 inch wafer. If the substrate is connected to the wafer using solder, then this solder connection would be required to compensate for the height variances in the substrate. Because of the geometries of the pads on the wafers, a maximum solder ball height of approximately .01 inch is possible. Therefore, only those solder bumps that resided on the highest part of the substrate would make contact with the wafer.

In the above example, the coplanarity of the substrate would have to be less than .00125 in./in. (.01 in across 8 inches) in order for all pads of the wafer to be contacted by the substrate. This requirement increases the cost of the substrate. As geometries become tighter, solder bump height decreases. Wafers are also becoming larger (e.g. 300mm = 12 inches across). These two factors increase the coplanarity or flatness requirements of the substrate which increases the cost of the substrate.

The invention described here overcomes the coplanarity problem by building the interposer onto the wafer. The substrate material is malleable at the time that it is placed on the wafer. Therefore, it can be urged against all contact pads on the wafer. Later, the entire assembly is cured. During the cure process solder contacts are made. Additionally, the underfill used to stabilize the assembly is cured at this time.

DESCRIPTION OF THE INVENTION:

Figure 1 shows the topside of a substrate 10. There are contact pads on both sides of the substrate. The pads that will contact the wafer are on the bottom and are not shown in Figure 1. These pads on the bottom are arranged to be in a mirror image of the pads on the wafer. They will typically have smaller geometries and tighter pitches than the pads shown on the top.

Figure 1 shows contact pads 11 that connect to four individual circuits 12 or die on the wafer. Each die has nine pads. Each contact pad on the bottom of the substrate 10 is connected to a pad 11 on the topside of the substrate. Although Figure 1 shows a die with nine pads, an actual semiconductor die may have many more individual contact pads (as many as 2000 or more). The pads 11 on the topside are constructed in an array with geometries larger than the pads on the bottom. This is done to enable easy contact with external burn-in or electrical test equipment. It also allows the use of less expensive printed circuit boards for attachment of individual circuits after the circuits have been fully processed and diced.

It is important to note that the substrate of Figure 1 has not been attached to the wafer. The material of the substrate is a laminate containing partially cured resins. This is often referred to as "B stage" laminate. The conducting pads on the top and bottom of the substrate can be copper, gold or other suitable conductive metal. They can also be a compound of different metals.

Figure 2 shows a wafer prepared for connection to the substrate. Solder bumps 21 have been applied to wafer 20. There will be one unique solder bump for each contact pad on the wafer. The solder bump may be applied directly to the die contact pad. Often the die pad will require additional layers of metal to be applied prior to the application of the solder bump. This is necessary to insure that the solder bump makes a strong and reliable connection to the die pad.

Additional metalization may be added to the wafer prior to the application of the solder bumps that redistribute the die contact pads. This is often necessary if the die pads have very small geometries or very close pitches. The redistributed pads help ensure that the solder connections made between the wafer and the substrate are robust and reliable.

Also shown in Figure 2 is no flow underfill 22. The purpose of this underfill is to stabilize the assembly by resisting any lateral forces caused by the differences between thermal expansion of the wafer and the substrate. The underfill is applied over the entire wafer but is not cured.

Figure 3 shows the substrate and the wafer prior to assembly into a wafer interposer. At this point the substrate 10 still contains partially cured resins. The solder bumps 21 have been applied to the contact pads of each die on wafer 20, The no flow underfill 22 is not cured at this step.

Prior to assembly, the wafer 20 is placed on a flat surface 31. The wafer is held in place by vacuum or other suitable technique. The substrate 10 is also held in place against a flat surface 32. A suitable compound is used to coat the surface of the substrate 10 that is in contact with the flat surface 32. This prevents the substrate from adhering to the flat surface during the curing process. Flat surfaces 31 and 32 as illustrated in Figure 3 can be various configurations and materials. The primary requirement of the surface is that it is as coplanar as the wafer. Also, not shown is a mechanism that can bring the surfaces together. This mechanism will be obvious to those skilled in the art. The mechanism must be able to adjust the position of the substrate or the wafer in order to perfectly align the contact pads on the substrate 10 with the solder bumps 21 on the wafer 20. Alignment is accomplished using split vision optics or any other suitable technique.

Prior to final assembly, the flat surface 32 may be heated to insure that the substrate 10 is in a malleable condition. The heating can be accomplished using forced heated air, heating coils or other method generally known in the industry.

Figure 4 shows the interposer assembly during assembly. Flat surfaces 32 and 31 are brought together by mechanical mechanisms not shown such that all solder bumps 21 contact the pads on substrate 10. A method for insuring that 100% contact is made is to compress the solder bumps. For example, if the solder bump is nominally .006 in. high, then the surfaces would be brought together such that the resulting solder bump would only be .005 in. high. This would compensate for any and all variances in the coplanarity of the substrate, wafer, solder bumps and flat surfaces.

Another method of manufacture includes applying underfill and solder bumps to the substrate instead of the wafer. Additionally, underfill and solder bumps may be applied to both the wafer and the substrate. The particular geometries of the contact pads or characteristics of the wafer or substrate would dictate the preferred method.

Figure 5 shows a "before" and "after" example of the effect of compression to make 100% connection. Before compression takes place, solder bumps 50a and 50b are not making contact with substrate 10. If the entire assembly were cured at this stage, missing connections would be present. Bringing the flat surfaces closer together results in the "after" configuration in Figure 5. Here, solder bumps 50a and 50b are making contact with substrate 10. The other solder bumps are compressed to allow 50a and 50b to contact the substrate. As they are compressed, solder must expand as height is reduced. This is possible because the surrounding underfill is not yet cured. The amount of compression to be applied will vary with each individual application.

After the wafer and substrate are properly joined, the entire assembly is cured. This curing can take place while the assembly continues to be held by the flat surfaces. Alternatively, the wafer and substrate may be removed from the surfaces and cured. During the curing process, the substrate and underfill become fully cured. In addition, the solder bumps make permanent contact with the contact pads. After the curing process, testing, burn-in or other processes designed to determine the merit of each circuit may be performed. The last step is dicing the assembly into individual circuits.

The invention described uses solder as a method of achieving connection. Other materials such as conductive polymer, conductive plastic or other suitable conductive material may be used.

The interposer may also be constructed by adding additional layers of substrate. This may be necessary to achieve thicker packages or to add additional interconnect options such as power and ground planes.

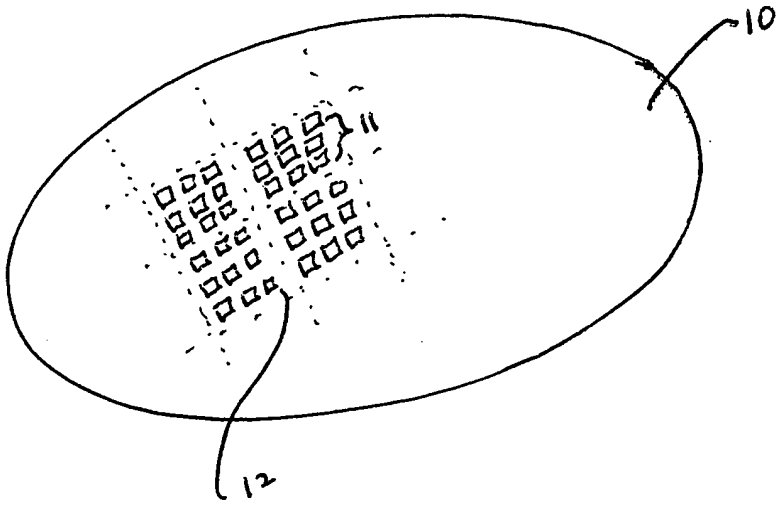


FIGURE 1

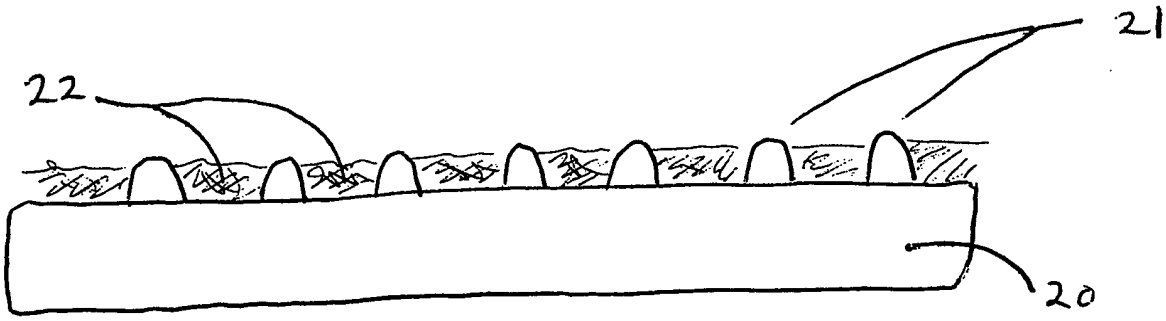


FIGURE 2

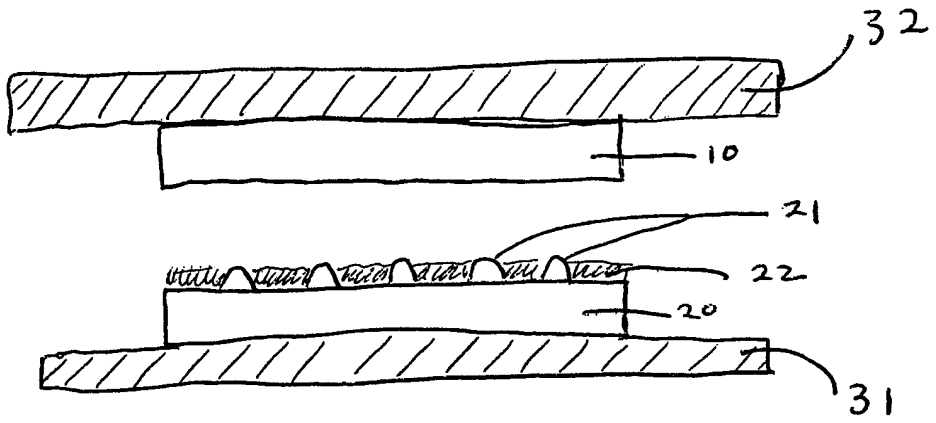


FIGURE 3

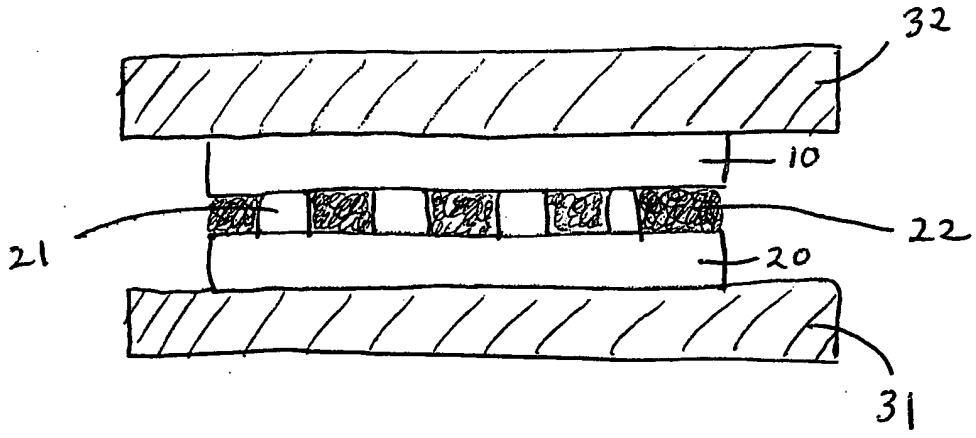
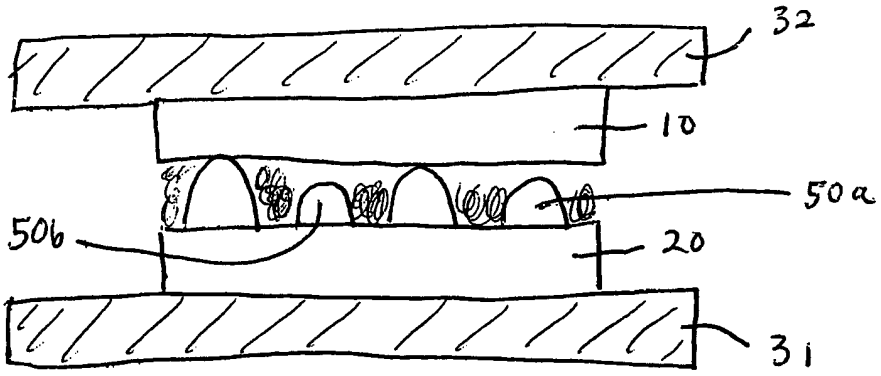
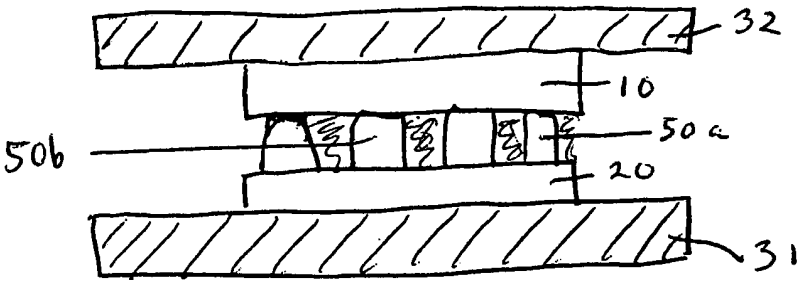


FIGURE 4



BEFORE



AFTER

FIGURE 5